REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application. Claims 1-6 are currently pending in this application. No new matter has been added by way of the present amendment. For instance, claims 1 and 2 have been amended to more clearly recite the novel features of the present invention. These amendments are non-narrowing in nature. Accordingly, no new matter has been added.

In view of the amendments and remarks herein, Applicants respectfully request that the Examiner withdraw all outstanding rejections and allow the currently pending claims.

Issues Under 35 U.S.C. § 102(b)

Claims 1-3 and 5 stand rejected under 35 U.S.C. 102(b) as being anticipated by Kashima et al. (JP 07-86162) (hereinafter Kashima '162). Applicants respectfully traverse.

The Examiner asserts that Kashima '162 discloses a method of forming a heterostructure film comprising supplying a group "IIIa" and "Va" material, so as to grow a "IIIaVa" thin film using gas source molecular beam epitaxy. The Examiner asserts that this step "reads on" Applicant's step of irradiating a molecular beam of at least one group III element and a molecular beam of a first group V element to form a first compound semiconductor layer.

The Examiner further asserts that Kashima '162 discloses that the supply of the "Va" group material is suspended and "t2 time discontinuation of the supply of all thin film raw materials to a substrate is carried out to terminate growth of the IIIaVa thin film". The Examiner argues that this step is similar to Applicant's step of stopping the irradiation of the molecular beam of the group III element and the molecular beam of the first group V element to halt growth until an amount of the

first group V element supplied is reduced to 1/10 or less, and asserts that "Kashima et al. teaches a time period t2 where all raw materials are suspended which reads on reducing a supply of the first group V element to 0."

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of anticipation. For anticipation under 35 U.S.C.§102, the reference must teach each and every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993). To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present". *In re Robertson*, 169 F.3d 743, 49 USPQ2d 1949 (Fed. Cir. 1999). The mere fact that a certain thing may result from a given set of circumstances is not sufficient. *Id.*

The present invention is directed, *inter alia*, to an epitaxial growth method to form a semiconductor thin film including a heterojunction of a group III-V compound semiconductor by means of molecular beam epitaxy. Present claim 1 requires a first step of irradiating a molecular beam of at least one of group III elements and a molecular beam of a first group V element to form a first compound semiconductor layer, a second step of stopping the irradiation of the molecular beam of the group III element and the molecular beam of the first group V element and halting growth for a period of time until the molecular beam intensity of the first group V element is reduced to 1/10 or less of that in the first step, and a third step of irradiating a molecular beam of at least one of the group III elements and a molecular beam of a second group V element to form an etch stopper layer on the first compound semiconductor layer.

Present claim 2 requires first and third steps as above, and further requires a second step of stopping the irradiation of the molecular beam of the group III element and the molecular beam of the first group V element and irradiating a molecular beam of a second group V element and halting growth for a period of time until the molecular beam intensity of the first group V element is reduced to 1/10 or less of that in the first step. Applicants submit that the prior art of record fails to explicitly or implicitly disclose a method as claimed.

Kashima '162 discloses an epitaxial growth method comprising: supplying a group III element and a first group V element ("Va") to form a first semiconductor layer; suspending the supply of the "Va" element temporarily; and, supplying a second group V element ("Vb"). The Examiner appears to interpret the presently claimed "second step" (see claims 1 and 2) as merely requiring discontinuation of the supply of element Va. However, Applicants submit that the Examiner's position is based on a misunderstanding of the present claims. The presently claimed "second step" in claims 1 and 2 and dependent claims thereof requires that irradiation be stopped when the concentration of the Va element is 1/10 or less of the initial concentration of this element (with the initial concentration being that in the "first step"). Kashima '162 does not teach a step of stopping the irradiation to halt growth until the molecular beam intensity of the first group V element is reduced to 1/10 of that in the first step.

The Examiner's attention is directed to the enclosed English "Translation of Written Reply", submitted in connection with PCT/JP2004/006144. Applicants note that the Examiner of the International Phase application admitted patentability of the present invention over Kashima '162.

As discussed in the enclosed Written Reply, the present method is an epitaxial growth method capable of forming a heterointerface with stable properties and forming an etch stopper layer with high selectivity. The present invention is characterized in that the time to start the growth of the second compound semiconductor layer (halt time) is determined based on a change in intensity of the molecular beam of the first group V element.

In a preferred embodiment of the present invention, growth is halted until the intensity of the group V molecular beam is reduced to 1/10 of the intensity of the group V molecular beam in the first step. Thereafter, an etch stopper layer is grown. As a result, the etching rate of the etch stopper layer is significantly lower in the present invention as compared to the etching rate of layers formed by conventional methods, as the amount of group V element mixed in the composition is lower.

The etching resistance of the etch stopper layer composed of the second compound semiconductor layer depends on the amount of the first group V element mixed therein. Applicants have discovered that unexpected and superior results are obtained when the growth of the etch stopper layer is started after the intensity of the group V molecular beam is reduced to 1/10 or less.

Kashima '162 includes no description or suggestion with regard to the etching resistance of the second compound semiconductor layer. Accordingly, even if the halt time in Kashima '162 was set based on the amount of the group V element supplied after the irradiation of the molecular beam is stopped, it would still not be possible to increase the etching resistance of the second compound semiconductor layer at all times.

Clearly, Kashima '162 fails to explicitly or implicitly teach each and every aspect of the claimed invention, and thus fails to anticipate the same. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Issues Under 35 U.S.C. § 103(a)

Claims 4 and 6 stand rejected under 35 U.S.C. 103(a) as being obvious over Kashima '162 in view of Watanabe (U.S. 6,229,162) (hereinafter Watanabe '162). Applicants respectfully traverse.

The Examiner admits that Kashima '162 does not teach a first layer of InP or InGaP and a second layer of InA1As or InGaAs. The Examiner, however, relies on the teachings of Watanabe '162 to overcome this deficiency.

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Additionally, there must be a reason why one of ordinary skill in the art would modify the reference or combine reference teachings to obtain the invention. A patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l Co. v Teleflex Inc.*, 82 USPQ2d 1385 (U.S. 2007). There must be a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. *Id.* The Supreme Court of the United States has recently held that the "teaching, suggestion, motivation test" is a valid test for obviousness, albeit one which cannot be

too rigidly applied. *Id.* Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *Id.*

As discussed above, Kashima '162 fails to teach an epitaxial growth method to form a semiconductor thin film including a heterojunction of a group III-V compound semiconductor by means of molecular beam epitaxy, comprising a first step of irradiating a molecular beam of at least one of group III elements and a molecular beam of a first group V element to form a first compound semiconductor layer, a second step of stopping the irradiation of the molecular beam of the group III element and the molecular beam of the first group V element and halting growth for a period of time until the molecular beam intensity of the first group V element is reduced to 1/10 or less of that in the first step, and a third step of irradiating a molecular beam of at least one of the group III elements and a molecular beam of a second group V element to form an etch stopper layer on the first compound semiconductor layer. Watanabe '162 fails to cure these deficiencies.

Watanabe '162 is directed to a high-speed, high-sensitivity planar-type avalanche photodiode. Watanabe '162 does not teach or suggest an epitaxial growth method as presently claimed.

Evidently, the cited references, alone or in combination, fail to teach or suggest every limitation of the instant invention. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and objections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action and, as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Marc S. Weiner, Reg. No. 32,181 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.147; particularly, extension of time fees.

Dated: JUL 09 2008

Respectfully submitted,

#32868

By _____
Marc S. Weiner
Registration No.: 32,181
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

Enclosure: Written Reply filed in connection with PCT/JP2004/006144, and English Translation thereof

MSW/VP/sh

WRITTEN REPLY

To: Mr. Kenichiro HASHIMOTO, examiner of Patent Office

1. International Application Number

PCT/JP2004/006144

2. Applicant

(*Omitted*)

3. Agent

(*Omitted*)

4. Date of Notice

August 31, 2004 (date of mailing)

5. Contents of Reply

In the opinions, the examiner found that the invention according to claim 1 did not involve an inventive step citing the Reference 1 (JP7-86162 (Hitachi, Ltd.) March 31, 1996) and found that the inventions according to claims 1 and 3 did not involve an inventive step citing the Reference 2 (JP6-97097 (NEC Corporation), April 8, 1994).

In order to make clear differences from the inventions described in the cited References, the attached amendment is filed to amend claims 1 and 2. Hereinafter, a description is given of findings based on the amended claims.

Concretely, "a third step of irradiating a molecular beam of at least one of the group III elements and a

molecular beam of a second group V element to form a second compound semiconductor layer, which is different from the first compound semiconductor, on the first compound semiconductor layer" (Claim 1, lines 8-10) is amended as follows: "a third step of irradiating a molecular beam of at least one of the group III elements and a molecular beam of a second group V element to form an etch stopper layer composed of a second compound semiconductor layer, which is different from the first compound semiconductor, on the first compound semiconductor layer." This makes it clear that the second compound semiconductor layer serves as the etch stopper layer. The above amendment is based on the description in lines 10-13 on page 8 of the specification.

For claim 1 before the amendment, the examiner found: "the Reference 1 does not clearly describe whether or not the growth of the laminate film is halted until an amount of As supplied is reduced to 1/10 or less of that at the growth of InGaAs. However, in the invention disclosed in the Reference 1, the film growth is halted in order to prevent the thin film materials from being mixed in the heterointerface. Accordingly, in the invention disclosed in the Reference 1, setting the halt time based on the amount of As supplied after the irradiation of the molecular beam is stopped can be readily thought of by those skilled in the art. Moreover, the value of 1/10 or less cannot be considered to have a critical significance."

As the examiner found, the technical method of halting the film growth in order to prevent the thin film materials from being mixed in the heterointerface and thus growing a heterostructure thin film having an extremely sharp heterointerface of good quality can be said to be a technology similar to the invention of the application.

However, the invention of the application is thought to differ from the invention according to the cited Reference 1 in that the above halt time is defined further in consideration of the etching resistance of the etch stopper layer composed of the second compound semiconductor layer.

Specifically, the invention of the application has been made focusing attention on the amount of group V element remaining at change of the group V element in the epitaxial growth by MBE and is an epitaxial growth method capable of forming a heterointerface with stable properties and "forming the etch stopper layer with high selectivity". The invention of the application is characterized in that the time to start the growth of the second compound semiconductor layer (or the halt time) is determined using a change in intensity of the molecular beam of the first group V element as an index based on the experimental results that the second compound semiconductor layer provides good etching resistance when the reduction ratio is not more than a certain limit (not more than 1/10), the

reduction ratio being a comparison between the intensity of the molecular beam of the first group V element (for example, As) when the growth of the first compound semiconductor layer has been completed and the intensity of the same when the growth of the second compound semiconductor layer is started.

Concretely, in the best mode for carrying out the invention, the growth is halted until the intensity of the As molecular beam is reduced to 1/10 of the intensity of the As molecular beam in the step a (for example, 30 sec) (step b). Thereafter, the InP etch stopper layer 30 is started to grow. The etching rate of the InP layer 30 is therefore 0.06 nm/sec, and the amount of As mixed is 0.025 in the composition (lines 8-10 on page 8). On the other hand, the etching rate of the InP layer formed by the conventional art is 0.15 nm/sec, and the amount of As mixed is 0.084 in the composition (lines 26-28 on page 8).

In other words, the etching resistance of the etch stopper layer composed of the second compound semiconductor layer depends on the amount of the first group V element mixed. When the mixed amount is not more than 0.05 in the composition, the etching rate is not more than 0.05 nm/sec. Herein, to make the amount of As mixed not more than 0.05 in the composition, it is necessary to start the growth of the InP etch stopper layer after the intensity of the As molecular beam is reduced to 1/10 or less. This provides a

critical significance in reducing the intensity of the As molecular beam to 1/10 or less.

The Reference 1 includes no description or suggestion about the etching resistance of the second compound semiconductor layer. Accordingly, in the invention disclosed in the Reference 1, even if the halt time is set based on the amount of As supplied after the irradiation of the molecular beam is stopped, the etching resistance of the second compound semiconductor layer cannot be always increased. It is therefore thought that the invention according to claim 1 of the application, which includes a requirement to halt the growth until the amount of the first V group element supplied is reduced to 1/10 or less of that in the first step in order to increase the etching resistance of the second compound semiconductor layer, cannot be easily conceived based on the invention described in the Reference 1.

Moreover, the examiner found as follows: "each of the inventions according to claims 2 to 4 does not involve an inventive step based on the Reference 2. The Reference 2 discloses a technology to prevent As from being mixed into the InP film at growing the InGaAs and InP laminate films using MBE by stopping the irradiation of the In, Ga, and As molecular beams while starting the irradiation of the P molecular beam and then irradiating the In molecular beam to grow the InP film."

However, the invention described in the Reference 2 is a technology of forming a group III metal layer in an interface to prevent As from being mixed into the InP film formed thereon and is recognized as a technical method different from that of the invention of the application. The Reference 2 includes no description or suggestion in terms of the etching resistance of the second compound semiconductor layer (InP film). Accordingly, in the invention disclosed in the Reference 2, even if the halt time is set based on the amount of As supplied after the irradiation of the molecular beam is stopped, the etching resistance of the second compound semiconductor cannot always be increased. It is therefore thought that the invention according to claim 2 of the application, which includes a requirement to halt the growth until the amount of the first V group element supplied is reduced to 1/10 or less of that in the first step, cannot be readily conceived based on the invention described in the Reference 2.

As described above, the contents in the scope of the inventions according to claims 1 and 2 of the application are that the aforementioned condition is a condition to determine the time factor of the growth program after the supply of the first group V element is stopped regardless of whether the second group V element starts to be supplied. Such a requirement cannot be readily thought of based on the invention described in the References 1 and 2.

Consequently, it is thought that each of claims 1 and 2 involves an inventive step. Moreover, it is convinced that each of claims 3 and 4, which technically limit claims 1 and 2, also involves an inventive step.

These are our findings to the opinions.

答　弁　書

特許庁審査官　　橋本　憲一郎 殿

１．国際出願の表示

ＰＣＴ／ＪＰ２００４／００６１４４

２．出願人

名　称　株式会社日鉱マテリアルズ

NIKKO MATERIALS CO., LTD

あて名　１０５－８４０７日本国東京都港区虎ノ門二丁目１０番１号

10-1, Toranomon 2-chome, Minato-ku, Tokyo 105-8407 Japan

国　籍　日本国　Japan

住　所　日本国　Japan

３．代理人

氏　名 (9003)弁理士　荒船　博司

ARAFUNE Hiroshi

あて名　１６２－０８３２日本国東京都新宿区岩戸町１８番地

日交神楽坂ビル５階

5F, Nikko Kagurazaka Building, 18, Iwato-cho, Shinjuku-ku,

Tokyo 162-0832 Japan

４．通知の日付　　３１．８．２００４（発送日）

５．答弁の内容

この度の見解書におきまして、審査官殿は、文献１（JP7-86162（株式会社日立製作所), 1995.03.31）を引用して請求の範囲１，３に記載の発明は進歩性を有さない、文献２（JP6-97097(日本電気株式会社), 1994.04.08 ）を引用して請

求の範囲２－４に記載された発明は進歩性を有さない旨の認定をされました。

そこで、引用文献に記載の発明との差異を明確にするため別紙補正書を提出して請求の範囲第１，２項を補正致しました。以下、補正後の請求の範囲に基づいて所見を申し述べます。

具体的には、請求の範囲第１項の８－１０行目に、「少なくとも一種類以上のＩＩＩ族元素の分子線と第２のＶ族元素の分子線とを照射して前記第１の化合物半導体層上に前記第１の化合物半導体とは異なり第２の化合物半導体層を形成する第３の工程と、」とあるのを、「少なくとも一種類以上のＩＩＩ族元素の分子線と第２のＶ族元素の分子線とを照射して前記第１の化合物半導体層上に前記第１の化合物半導体とは異なり第２の化合物半導体層からなるエッチストッパー層を形成する第３の工程と、」と補正し、第２の化合物半導体層はエッチストッパー層となることを明確にしました。かかる補正は明細書第８頁第１０－１３行目等の記載を根拠とします。

補正前の請求の範囲第１項に対して、貴官は、「文献１には、Ａｓの供給量がＩｎＧａＡｓの成長時の１／１０以下となるまで積層膜の成長を中断しているか否かについては明記されていないが、文献１に開示された発明は、ヘテロ界面における薄膜原料の混合を防ぐために膜の成長を中断しているのであるから、文献１に開示された発明において、分子線の照射停止後のＡｓの供給量に基づいて中断時間を設定することは、当業者が容易になし得たに過ぎない。そして、１／１０以下なる値に臨界的意義があるとも認められない。」と認定されています。

審査官が認定されたとおり、ヘテロ界面における薄膜原料の混合を防ぐために膜の成長を中断し、極めて急峻で良質なヘテロ界面を有するヘテロ構造薄膜を成長させるという技術的手法は、本願発明と類似する技術であるといえます。

しかしながら、本願発明では、さらに、第２の化合物半導体層からなるエッチストッパー層のエッチング耐性を考慮して、上記中断時間を規定している点で引用文献１に記載の発明とは相違すると思料します。

すなわち、本願発明は、ＭＢＥ法によるエピタキシャル成長におけるＶ族元素の切換時の残留Ｖ族元素量に着目してなされたもので、安定した特性を有するヘテロ界面の形成できるとともに、『高い選択性をもったエッチストッパー層の形

成を実現する』エピタキシャル成長方法です。そして、第１の化合物半導体層成長完了時点における第１のＶ族元素（例えばＡｓ）の分子線強度と、第２の化合物半導体層の成長開始時点における第１のＶ族元素の分子線強度を比較した減少率が一定限度以下（１／１０以下）の場合に、第２の化合物半導体層のエッチング耐性が良好になるという実験結果に基づいて、第１のＶ族元素の分子線強度の変化を指標として第２の化合物半導体層の成長開始時点（或いは中断時間）を決定する点を特徴とします。

具体的には、発明を実施するための最良の形態において、Ａｓ分子線強度が工程ａにおけるＡｓ分子線強度の１／１０（例えば３０ｓｅｃ）だけ成長を中断させた後に（工程ｂ）、ＩｎＰエッチストッパー層３０の成長を開始することで、ＩｎＰ層３０のエッチング速度は０．０６ｎｍ／ｓｅｃ、Ａｓ混入量は組成にして０．０２５となります（第８頁第８－１０行目）。これに対して、従来技術により形成されたＩｎＰ層のエッチング速度は０．１５ｎｍ／ｓｅｃ、Ａｓ混入量は組成にして０．０８４となります（第８頁第２６－２８行目）。

つまり、第２の化合物半導体層からなるエッチストッパー層のエッチング耐性は、混入される第１のＶ族元素の混入量に依存し、その混入量が組成にして０．０５以下であればエッチング速度は０．０５ｎｍ／秒以下となります。ここで、Ａｓ混入量を組成にして０．０５以下とするためには、Ａｓ分子線強度が１／１０以下となった後にＩｎＰエッチストッパー層の成長を開始させることが必要となりますので、ここにＡｓ分子線強度を１／１０以下にすることの臨界的意義を認めることができます。

また、文献１には第２の化合物半導体層のエッチング耐性については記載も示唆もされていませんので、文献１に開示された発明において、分子線の照射停止後のＡｓの供給量に基づいて中断時間を設定したとしても、必ずしも第２の化合物半導体層のエッチング耐性を向上できるとは限りません。したがって、第２の化合物半導体層のエッチング耐性を向上させるために第１のＶ族元素の供給量が第１の工程における供給量の１／１０以下となるまで成長を中断することを要件とした本願請求項１に係る発明は、文献１に記載の発明に基づいて容易に想到できるものではないと思料します。

また、貴官は、「請求の範囲２－４に記載された発明は、文献２から進歩性を有さない。文献２には、分子線エピタキシーを用いて、ＩｎＧａＡｓとＩｎＰの積層膜を成長させる際に、Ｉｎ，Ｇａ，Ａｓの分子線の照射を停止するとともにＰの分子線の照射を開始し、その後にＩｎの分子線を照射してＩｎＰ膜を成長させることにより、ＩｎＰ膜へのＡｓの混入を防ぐ技術が開示されている。」と認定されています。

しかしながら、文献２に記載の発明は、界面にＩＩＩ族メタル層を形成することにより、その上に形成されるＩｎＰ膜へのＡｓの混入を防ぐ技術であり、本願発明とは技術手法として別のものであると認められます。また、文献２には、第２の化合物半導体層（ＩｎＰ膜）のエッチング耐性については記載も示唆もされていませんので、文献２に開示された発明において、分子線の照射停止後のＡｓの供給量に基づいて中断時間を設定したとしても、必ずしも第２の化合物半導体層のエッチング耐性を向上できるとは限りません。しがたって、本願請求項２に係る第１のＶ族元素の供給量が第１の工程における供給量の１／１０以下となるまで成長を中断することを要件とする本願請求項２に係る発明を文献２に記載の発明に基づいて容易に想到することはできないと思料します。

以上説明しましたように、本願請求項１，２に係る発明は、第１のＶ族元素の供給を停止した後、第２のＶ族元素の供給開始の如何を問わず、上記条件が成長プログラムの時間的要素を決める条件であることを請求の範囲の内容とするもので、かかる要件を文献１，２に記載の発明に基づいて容易に想到することはできませんので、本願請求項１，２は進歩性を有するものと思料します。また、請求項１または２を技術的に限定した請求項３，４についても同様に進歩性を有するものと確信します。

この度の見解書に対する所見は以上のとおりです。